

WHAT IS CLAIMED IS:

1. An SRAM device, comprising:

2 an SRAM array coupled to row peripheral circuitry by a word
3 line and coupled to column peripheral circuitry by bit lines; and
4 an array low voltage control circuitry that provides an
5 enhanced low operating voltage V_{ESS} to said SRAM array during at
6 least a portion of an active mode thereof.

2. The SRAM device as recited in Claim 1 wherein said array

2 low voltage control circuitry provides said enhanced low operating
3 voltage V_{ESS} only during a WRITE operation.

3. The SRAM device as recited in Claim 1 wherein said array

2 low voltage control circuitry provides said enhanced low operating
3 voltage V_{ESS} during all of said active mode.

4. The SRAM device as recited in Claim 1 wherein said array

2 low voltage control circuitry provides said enhanced low operating
3 voltage V_{ESS} during all modes.

5. The SRAM device as recited in Claim 1 wherein said array
2 low voltage control circuitry provides said enhanced low operating
3 voltage V_{ESS} based on a factor selected from the group consisting
4 of:

5 a process corner,
6 a transistor parameter,
7 a mode of operation, and
8 a value of a high supply voltage.

6. The SRAM device as recited in Claim 1 wherein said array
2 low voltage control circuitry provides said enhanced low operating
3 voltage V_{ESS} at a higher value when based on a strong n process
4 corner.

7. The SRAM device as recited in Claim 1 wherein said array
2 low voltage control circuitry provides said enhanced low operating
3 voltage V_{ESS} at a lower value during a READ operation than during a
4 WRITE operation.

8. The SRAM device as recited in Claim 7 wherein said array
2 low voltage control circuitry only provides said lower value for an
3 addressed column of said SRAM array.

9. The SRAM device as recited in Claim 1 wherein said array
2 low voltage control circuitry employs an active component to
3 provide said enhanced low operating voltage V_{ESS} .

10. The SRAM device as recited in Claim 1 wherein said array
2 low voltage control circuitry provides said enhanced low operating
3 voltage V_{ESS} employing a component selected from the group
4 consisting of:

5 a diode,
6 a transistor,
7 a fuse,
8 a ROM,
9 a voltage regulator, and
10 logic circuitry.

11. The SRAM device as recited in Claim 1 wherein said array
2 low voltage control circuitry provides said enhanced low operating
3 voltage V_{ESS} at a higher value than a low operating voltage V_{ss} .

12. A method of operating an SRAM device, comprising:

2 employing in an integrated circuit an SRAM array coupled to
3 row peripheral circuitry by a word line and coupled to column
4 peripheral circuitry by bit lines; and
5 providing an enhanced low operating voltage V_{ESS} to said SRAM
6 array during at least a portion of an active mode.

13. The method as recited in Claim 12 wherein said providing
2 only occurs during a WRITE operation.

14. The method as recited in Claim 12 wherein said providing
2 occurs during all of said active mode.

15. The method as recited in Claim 12 wherein said providing
2 occurs during all modes.

16. The method as recited in Claim 12 wherein said providing
2 is based on a factor selected from the group consisting of:
3 a process corner,
4 a transistor parameter,
5 a mode of operation, and
6 a value of a high supply voltage.

17. The method as recited in Claim 12 wherein said enhanced
2 low operating voltage V_{ESS} is provided at a higher value based on
3 a strong n process corner.

18. The method as recited in Claim 12 wherein said enhanced
2 low operating voltage V_{ESS} is provided at a lower value during a
3 READ operation than during a WRITE operation.

19. The method as recited in Claim 18 wherein said lower
2 value is only provided for an addressed column of said SRAM array.

20. The method as recited in Claim 12 wherein said providing
2 includes employing an active component to provide said enhanced low
3 operating voltage V_{ESS} .

21. The method as recited in Claim 12 wherein said providing
2 includes employing a component selected from the group consisting
3 of:

4 a diode,
5 a transistor,
6 a fuse,
7 a ROM,
8 a voltage regulator, and
9 logic circuitry.